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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,765	11/07/2001	Franck Roche	00RO30454288	9186

27975 7590 05/17/2010

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
05/17/2010	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FRANCK ROCHE and PIERRE TARAYRE

Appeal 2009-004532
Application 10/039,765
Technology Center 2100

Decided: May 13, 2010

Before LANCE LEONARD BARRY, CAROLYN D. THOMAS, DEBRA K. STEPHENS, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

The Patent Examiner rejected claims 20-46 and 48-52. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

INVENTION

The Appellants describe the invention at issue on appeal as follows.

> An object of the present invention is to provide a data transmission method that is of the synchronous type and which enables two devices with very different clock frequencies, where applicable, to communicate.
>
> Another object of the present invention is to provide such a synchronous method that can be implemented with only two wires or lines, for serial data transmission.

(Spec. 3-4.)

ILLUSTRATIVE CLAIM

> 20. A method of transmitting data between two devices via a clock line and at least one data line, the clock line being maintained by default on a first logic value, the method comprising:
>
> providing each device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value;
>
> tying the clock line to the second logic value, via the two devices, after data is applied to the data line;
>
> maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data; and
>
> maintaining the data on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent.

PRIOR ART

SPI Block Guide ("SPI"), V 3.06, Freescale Semiconductor, Inc., January 21, 2000.

System Management Bus Specification ("SMB"), Version 2.0, SBS Implementers Forum, August 3, 2000.

REJECTIONS

Claims 44-46 are rejected under 35 U.S.C. 102(a) as being anticipated by SPI.

Claims 51 and 52 are rejected under 102(a) as being anticipated by SMB.

Claims 20-43 and 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over SPI and SMB.

CLAIMS 44-46

Based on the Appellants' arguments, we will decide the appeal of claims 44-46 based on claim 44 alone. *See* 37 C.F.R. § 41.37(c)(1)(vii).

The Examiner makes the following findings.

> SPI discloses tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high) (Page 27, Figure 4-2, CPOL=1, SCK changes from 1(idle state) to 0 at SCK Edge Nr. 1); and waiting for the clock line to have the first logic value(CPOL=l, idle state, SCK=1), applying data to the data line(MOSI pin), tying the clock line to the second logic value(Figure 4-2, Data is applied before SCK Edge Nr. 1) . . . .

(Ans. 14.) The Appellants argue that "in FIG. 4-2, the clock line SCK alternates between the high and the low state (when CPOL=1) but does not teach or suggest how the clock signal SCK is controlled by the devices exchanging data." (App. Br. 17.)

ISSUE

Therefore, the issue before us is whether the Examiner has erred in finding that SPI discloses how a clock line is tied to a potential representing a second logic value of that is the opposite of a first logic value.

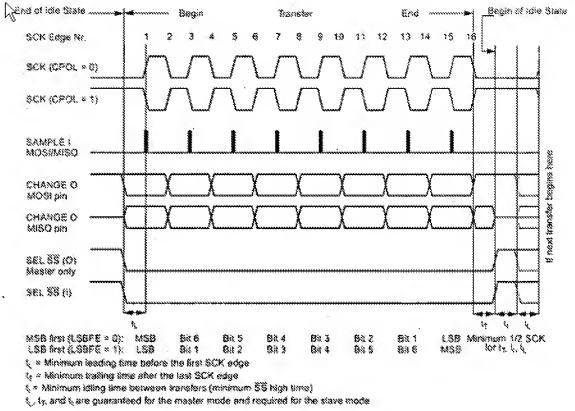
LAW

"It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim, and that anticipation is a fact question . . . ." *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) (citing *Lindemann Maschinenfabrik GMBH v. Am. Hoist & Derrick Co.,* 730 F.2d 1452, 1457 (Fed. Cir. 1984)). Furthermore, "[a]ll of the disclosures in a reference must be evaluated for what they fairly teach one of ordinary skill in the art." *In re Boe*, 355 F.2d 961, 965 (CCPA 1966)). "The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain.'" *In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) (quoting *In re Lemelson*, 397 F.2d 1006, 1009 (CCPA 1968)).

FINDINGS OF FACT

SPI teaches an SPI Control Register 1 (p. 16) featuring a "CPOL — SP1 Clock Polarity Bit" (p. 17). "This bit selects an inverted or non-inverted SPI clock." (*Id.*) More specifically, "1 = Active-low clocks selected. In idle state SCK is high." (*Id.*)

Figure 4-2 of the reference follows.



"Figure 4-2 is a timing diagram of an SPI transfer . . . ." (p. 27.)

The Appellants admit that SPI's "clock is entirely under the control of the master device which uses a Baud Rate Generator to emit the clock signal." (App. Br. 16.)

ANALYSIS

SPI teaches an SPI Control Register 1 featuring a CPOL — SPI Clock Polarity Bit. When the bit is set to 1, the SPI's clock ("SCK") is tied to a high value during the idle state of the SPI's system. The SCK (SPOL = 1) signal line of Figure 4-2 shows SCK being tied to an active high during the idle state.

The Appellants admit that SCK is under the control of the master device. Figure 4-2, moreover, shows that upon placing the leftmost bit of data on line "CHANGE 0 MOSI pin," the master device ties SCK to a low logic value of that is the opposite of a (high) idle logic value

CONCLUSION

Based on the aforementioned facts and analysis, we conclude that the Examiner has not erred in finding that SPI discloses how a clock line is tied to a potential representing a second logic value of that is the opposite of a first logic value.

CLAIMS 51 AND 52

Based on the Appellants' arguments, we will decide the appeal of claims 51 and 52 based on claim 51 alone.

The Examiner finds that "SMB discloses . . . a trigger for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value(Page 22, Section 4.3.3, The clock is stretched low periodically) . . . ." (Ans. 10.) The Appellants argue that "such a trigger is not disclosed because the SMBus Specification fails to teach or suggest tying the clock line to the second logic value, via two devices . . . ." (App. Br. 19.) They also argue that "[e]ven though the SMBus Specification discloses that a slave device may stretch the clock period, the slave must comply with a certain timeout." (*Id.*)

ISSUE

Therefore, the issue before us is whether the Examiner has erred in finding that SMB discloses tying a clock line to a logic value.

LAW

"[T]he PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)).

FINDINGS OF FACT

SMB (p. 22) includes the following disclosure.

> A slave device may opt to stretch the clock line during a specific bit transfer in order to process a real time task or check the validity of a byte. In this case the slave device must adhere to the $T_{TIMEOUT}$ and $T_{LOW:SEXT}$ specifications. Clock LOW extension may occur during any bit transfer including the clock provided prior to the ACK clock pulse.
>
> A slave device may select to stretch the clock LOW period between byte transfers on the bus, in order to process received data or prepare data for transmission. In this case the slave device will hold the clock line LOW after the reception and acknowledgement of a byte . . . .

ANALYSIS

Here, although the Appellants argue that SMB fails to teach tying its clock line to the second logic value via two devices, claim 51 does not

require tying *via two devices*. Furthermore, we will not read such a limitation into the claim when the Appellants could have recited it as they do in claim 20.

For its part, SMB does disclose that its slave device may stretch the clock line during a specific bit transfer to process a real time task or check the validity of a byte. We agree with the Examiner's finding that such a stretching constitutes tying a clock line to a logic value. We also agree with his following findings.

> SMB discloses that the slave must adhere to timeout parameter. This timeout enables the master or slave to conclude that a defective device is holding the clock low indefinitely(Page 13, Section 3.1.1.3). However, during normal operation, i.e. no defective devices, the slave can maintain the tie to the clock to stretch the low period of the clock and therefore meets the claim language. The claim language does not require devices without timeout values. Thus, Appellant[s]' argument is not persuasive.

(Ans. 14.)

CONCLUSION

Based on the aforementioned facts and analysis, we conclude that the Examiner has not erred in finding that SMB discloses tying a clock line to a logic value.

CLAIMS 20-43 AND 48-50

Based on the Appellants' arguments, we will decide the appeal of claims 20-43 and 48-50 based on claim 20 alone.

The Examiner makes the following findings.

> SPI discloses a device (master) provided with the ability to tie the clock to a potential representing a second logic value(SCK=Low=0) opposite of the first logic value at SCK Edge Nr. 1 (Figure 4-2) and SMB discloses a device(slave) with the ability to tie the clock to a potential representing a second logic value(SMBCLK=0) opposite of a first logic(SMBCLK=0) (Page 22, Section 4.3.3, Figure 4-7).

(Ans. 12.) The Appellants argue that "[t]he SMBus Specification fails to teach or suggest that both the master and the slave device can tie the clock line to a second logic value opposite the first logic value." (App. Br. 14.)

ISSUE

Therefore, the issue before us is whether the Examiner has erred in finding that the combined teachings of SPI and SMB would have suggested that both a master and a slave device can tie a clock line to a second logic value opposite a first logic value.

LAW

"The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art." *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)). "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *Keller*, 642 F.2d at 425). In determining obviousness, furthermore, a reference "must be read, not in isolation, but for what it fairly teaches in combination with the prior art as a whole." *Id.*

FINDINGS OF FACT

The Appellants admit that SMB's "master device can tie the clock line to a different potential." (App. Br. 14.)

ANALYSIS

Here, the Examiner's rejection of claim 20 is based on what the combined teachings of SPI and SMB would have suggested to one of ordinary skill in the art. The Appellants, however, attack SMB individually. Such an attack cannot establish non-obviousness.

Regarding claims 44-46, we have agreed with the Examiner's finding that SPI's master can tie a clock line to a second logic value opposite a first logic value. Furthermore, the Appellants admit that SMB's master device can tie the clock line to a different potential. Regarding claims 51 and 52, moreover, we have agreed with the Examiner's finding that SMB's slave device may tie a clock line to a logic value.

CONCLUSION

Based on the aforementioned facts and analysis, we conclude that the Examiner has not erred in finding that the combined teachings of SPI and SMB would have suggested that both a master and a slave device can tie a clock line to a second logic value opposite a first logic value.

DECISION

We affirm the rejection of claims 20-46 and 48-52.

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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